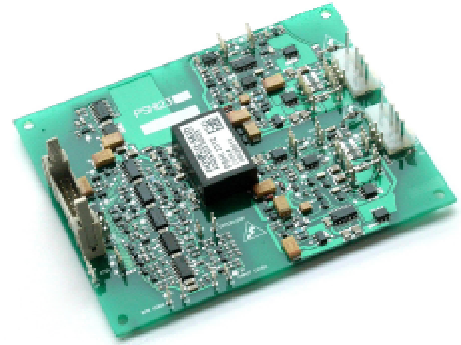


1. Absolute Maximum Ratings(Ta=25°C)

Symbol	Terms	Values	Units
V _S	Supply voltage primary	18	V
V _{iH}	Input signal voltage(HIGH)	V _S +0.3	V
I _{outPEAK}	Output peak current	±8	A
I _{outAV}	Output average current	±50	mA
V _{CE}	Collector-emitter voltage sense	1200 / 1700	V
dv/dt	Rate of rise and fall of voltage	75	kV/μs
V _{isol IO}	Isolation test volt.IN-OUT(1min.AC)	4000	V
R _{Gon min}	Minimal R _{Gon}	2.7	Ω
R _{Goff min}	Minimal R _{Goff}	2.7	Ω
Q _{out/pulse}	Charge per pulse	±4.8	μC
T _{op}	Operating temperature	-25~85	°C
T _{stg}	Storage temperature	-25~85	°C



**POWER-SEM
PCB IGBT Driver
PSHI 2312
PSHI 2317**

High Power Double IGBT Driver

Features

- PSHI 23/12 drives all series IGBTs with V_{CEs} up to 1200V(V_{CE}-monitoring adjusted from factory for 1200V IGBT)
- PSHI 23/17 drives all series IGBTs with V_{CEs} up to 1700V(V_{CE}-monitoring adjusted from factory for 1700V IGBT)
- Double driver circuit for medium power IGBTs, also as two independent single drives
- CMOS/TTL(HCMOS) compatible input buffers
- Short circuit protection by V_{CE} monitoring
- Soft short circuit turn-off
- Isolation due to transformers(no opto couplers)
- Supply undervoltage protection(<13V)
- Error memory/output signal (LOW OR HIGH LOGIC)
- Driver interlock top/bottom in half-bridge mode
- Internal isolated power supply
- Short-pulse control function

2. Electrical Characteristics (Ta=25°C)

Symbol	Terms	Values			Unit
		min	typ	max	
V _S	Supply voltage primary	14.4	15	15.6	V
I _S	Supply current(max.)		0.32 ¹⁾		A
I _{SO} ²⁾	Supply current primary side(standby)		0.12		A
V _{IT+}	Input threshold voltage(HIGH)min For 15V input level For 5V input level	12.5 2.4			V
V _{IT-}	Input threshold voltage(LOW)max For 15V input level For 5V input level			3.6 0.5	V
R _{In}	Input resistance		10		kΩ
V _{G(on)}	Turn-on output gate voltage		15		V
V _{G(off)}	Turn-off output gate voltage		-8		V
f	Maximum operating frequency		see Fig.1		
t _{d(on)IO}	Input-output turn-on propagation time		1.4		μs
t _{d(off)IO}	Input-output turn-off propagation time		1.4		μs
t _{d(er)}	Error input-output propagation time		1 ³⁾		μs
V _{CEstat}	Reference voltage for V _{CE} monitoring		5.2 ⁴⁾ /6.3 ⁵⁾		V
C _{PS}	Primary to secondary capacitance		12		Pf

- 1) This current value is a function of the output load condition
- 2) Operating fsw=0Hz
- 3) This value is not considered by t_{on} and t_{dead} of IGBT, but adjusted by R_{CE} and C_{CE}
- 4) With R_{CE}=18k Ω, C_{CE}=330pF(PSHI2312 used for 1200V IGBT)
- 5) With R_{CE}=36k Ω, C_{CE}=470pF(PSHI2317 used for 1700V IGBT)

Typical Applications

- Single and bridge circuit
- Inverter
- Welding machine
- induction heating
- High power UPS
- High frequency SMPS

3. Product Overview

The new intelligent double IGBT driver, PSHI2312 respectively PSHI2317 is a standard driver for all power IGBTs in the market. PSHI2312 drives all IGBTs with V_{CE} up to 1200V. PSHI2317 drives all IGBTs with V_{CE} up to 1700V. Power-sem PSHI23 driver series are able to be compatible with those of Semikron's completely. To protect the driver against moisture, dust, it is coated with varnish. The adaption of the drivers to the application has been improved by using pins to changing several parameters and functions, different types of IGBT can be drove easily by adjusting R_{Gon} , R_{Goff} and $R_{Goff-sc}$ value. The connections to the IGBTs can be made by using 2 separate connectors with 5 pins for each IGBT. The high power outputs capability was designed to switch high current double or single modules (or paralleled IGBTs). The output buffers have been improved to make it possible to switch up to 200A IGBT modules at frequencies up to 20kHz. High power output can be achieved by paralleling more IGBTs. A new function has been added to the short circuit protection circuit (Soft Turn Off), this automatically increases the IGBT turn off time and hence reduces the DC voltage overshoot enabling the use of higher DC-bus voltages. This means an increase in the final output power. Integrated DC/DC converters with high galvanic isolation (4kV/1 minute) ensures that the user is protected from the high voltage (secondary side). The power supply for the driver may be the same as used in the control board (0/+15V) without the requirement of isolation. All information that is transmitted between input and output uses ferrite transformers, resulting in high dv/dt immunity (75kV/ μ s) which has high anti-jamming ability. The driver input stages integrated a input level selector (15V/5V input level), which suitable for different output level of control board.

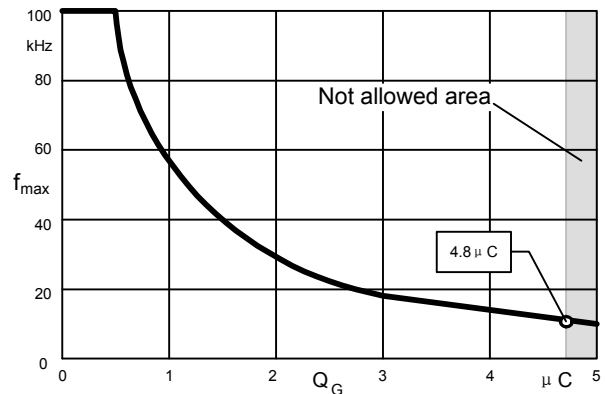


Fig.1 Relationship between maximum operating frequency and charge per pulse

4. Block diagram PSHI 23

System structure features (see Fig 2)

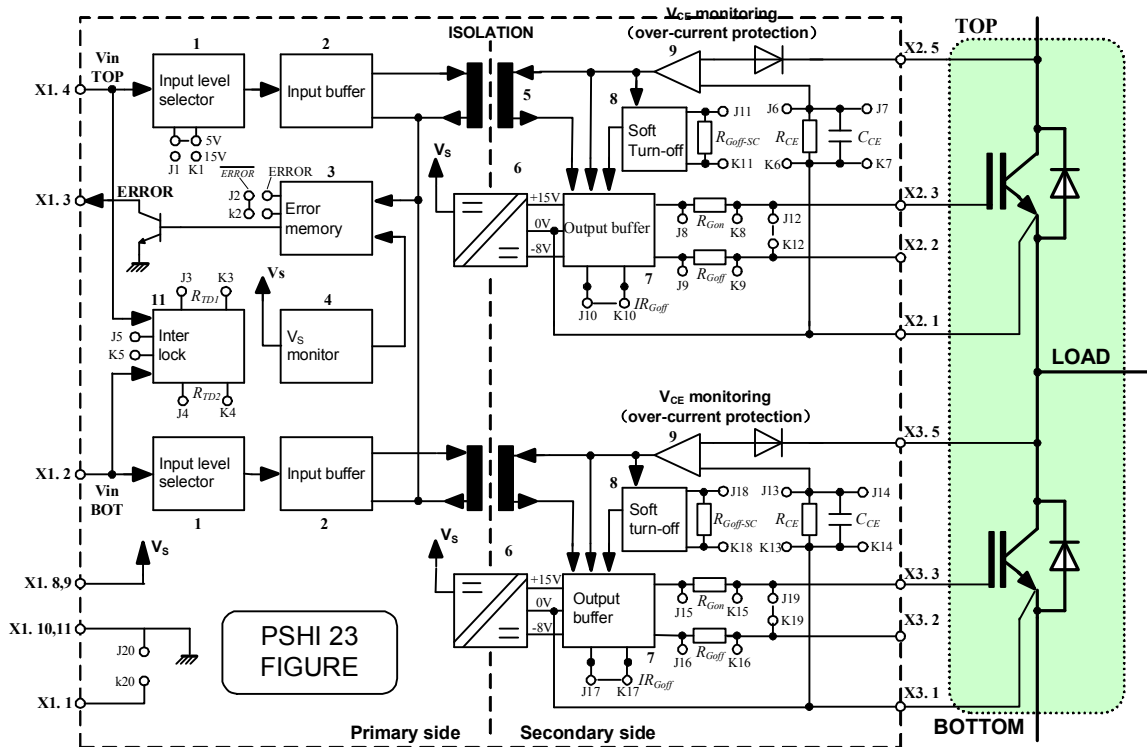
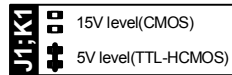


Fig.2 System structure of PSHI 23

System structure and performance features:

■ “INPUT LEVEL SELECTOR” circuit can choose 5V (TTL,HCMOS) or 15V (CMOS) signal. By comparing a signal with a level, it fix input signals and enhance improve driver’s anti-jamming ability. COMS is adjusted from factory for 15V, but can be changed by the user to 5V HCMOS level by solder bridging between J1 and K1. The standard level is +15V (factory adjusted) intended for noisy environments or when long connections (L>50cm) between the external control circuit and PSHI 23 are used, where noise immunity must be considerate. For lower power, and short connections between control board and driver, the TTL - HCMOS level (+5V) can be selected by solder bridging between J1 and K1, specially useful for signals from uP based controllers.



When connecting PSHI23 to control board using short connecting lead, no special attention needs to be taken. Otherwise, if the length is 50cm or more (we suggest to limit the cable length to about 1 meter), some care must be taken. The TTL (5V) level should be avoided and CMOS(15V) is to be used instead; flat cable must have the pairs of conductors twisted or be shielded cable is used, it can be connected to pins J20 & K20 and x1.1 coupled to ground through a capacitor, resistor or jumper.

5V level is not commended to be used for long input cable because of existing interference.

An internal pull-down resistor of driver signal inputs keeps the IGBT in OFF state in case V_{in} connection is interrupted or left non connected.

The following overview is showing the input threshold voltages:

VIT+ (High)	min	typ	max	VIT- (Low)	min	typ	max
15 V	9.5 V	11.0 V	12.5 V	15 V	3.6 V	4.2 V	4.8 V
5 V	1.8 V	2.0 V	2.4 V	5 V	0.50 V	0.65 V	0.80 V

■ An “INTERLOCK” circuit prevents the two IGBTs of the half bridge to switch-on at the same time, and a “dead time” (default:10us) can be adjusted by adjusting resistor value of pins J3 & K3, and J4 & K4, to suit for IGBTs with different current level and different operating frequency. Tab 1 shows the corresponding relationship between R_{TD} and dead time. The interlocking may also be inhibit by solder bridging between pins J5 and K5 to obtain two independent drivers(see Fig.3).

■ “INPUT BUFFER” circuit converts input signals in order to make them meet the needs of ferrite transformers and avoid other false signals being transmitted to output side.

■ The “ERROR MEMORY” blocks the transmission of all turn-on signals to the IGBT and output error signal by a OC transistor if either over-current or under-voltage is detected. Default error signal output is high level active, while needing low level active, just soldering bridged J2 with K2.

■ The “ V_s MONITOR” ensures that V_s actual is not below 13V. Once V_s below 13V, system will blocks the transmission of all input signals to the IGBT.

■ With a “FERRITE TRANSFORMER” the information between primary and secondary may flow in both directions and high levels of dv/dt (75kV/us) and high isolation voltage(AC4kV, 1 min.). At the same time, it can also restrain the short-pulse signals below 500ns.

■ A high frequency “DC/DC power supply” used in “power output circuit” to supply isolation power supply with output voltage: +15V/-8V. Power supply use full-bridge circuit, filtering and stablization, which make the driver get enough gate voltage without external isolation power supply. The drivers and controlled system can use same power supply(+15V), even if we are using more than one PSHI23.

■ In case of short-circuit, a further circuit (SOFT TURN-OFF) increases the resistance in series with R_{Goff} and turns-off the IGBT at a lower speed. This produces a smaller voltage spike (due to LSTRAY’ di/dt) above the DC link by reducing the di/dt value. Because in short-circuit conditions the Homogeneous IGBT’s peak current increases up to 6-8 times the nominal current, and some stray inductance is always present in power circuits, it must fall to zero in a longer time than at normal operation to avoid damage IGBT by high voltage spike. The default resistor used for soft turn-off is 22 Ω , this “soft turn-off time” can be reduced by connecting a parallel resistor $R_{Goff-SC}$ on J11, K11 & J18, K18 with those already on the printed circuit board(see Fig.4).

R_{TD} resitance value	Dead time
10 k Ω	0.9 μ s
22 k Ω	1.8 μ s
33 k Ω	2.5 μ s
47 k Ω	3.2 μ s
68 k Ω	4 μ s
100 k Ω	5 μ s
330 k Ω	7.7 μ s
not bridged	10 μ s

Tab 1. Corresponding relationship between R_{TD} and dead time

■ “ V_{CE} monitoring circuit” is responsible for short-circuit sensing. Due to the direct measurement of V_{CEstat} on the IGBT’s collector, it blocks the output buffer (through the soft turn-off circuit) in case of short-circuit and sends a signal to the ERROR memory on the primary side.

The reference voltage V_{CEref} adjusted dynamically according to IGBT switch characteristics, and reset when IGBT turn-off. The V_{CEref} is not static but a dynamic reference which has an exponential shape starting at about 15 V and decreases to V_{CEstat} (determined by R_{CE}), with a time constant τ (controlled by C_{CE}) (see Fig.5).

V_{CEsat} threshold is a static value of V_{CEref} which is controlled by resistor R_{CE} (see Fig.6a). It can be adjusted by resistor R_{CE} (J6,K6;J13,K13) to reach the maximum value as per IGBT’s demand. $V_{CEstat} > V_{CEsat}$ under normal conditions, but will not exceed 10V. The decay time of V_{CEref} is determined by capacitor C_{CE} and resistor R_{CE} (see Fig.6b). It controls the dead time t_{dead} when IGBT just starts to conduct till V_{CEsat} monitoring starts.

To avoid a false failure indication when the IGBT just starts to conduct ($V_{CE} > V_{CEref}$), some decay time t_{dead} must be provided for the V_{CEref} . As the V_{CE} signal is internally limited at 10 V, “ V_{CE} monitoring circuit” will be trigger and cut off IGBT by “soft turn-off circuit” when V_{CEref} drops to 10V (ie.leave monitor dead area t_{dead}) and V_{CE} voltage rises above the reference voltage at any time ($V_{CE} > V_{CEref}$). The various different operating conditions are depicted in Fig.7.

The monitor sensitivity of “ V_{CE} monitoring circuit” is adjusted by changing dead time t_{dead} . This can be realized by extending monitoring dead area via adjusting C_{CE} (J7,K7;J14,K14) under certain applications, such as TOP & BOT IGBT connected instantly. Please make sure the total time from IGBT conduct (start from short circuit) to IGBT totally turn-off by soft turn-off circuit must shorter than IGBT safe short circuit time (usually 10us or 6us, details pls refer to IGBT supplier). The total time includes $t_{dead} + t_{d(Err)} + t_{off-SC}$, IGBT turn-off trailing time and safety time.

PSHI 2312 driver with $R_{CE} = 18k \Omega$, $C_{CE} = 330pF$ adjusted from factory.

PSHI 2317 driver with $R_{CE} = 36k \Omega$, $C_{CE} = 470pF$ adjusted from factory. (see Fig.4 curve 2)

Attention: If this function is not used, for example during the experimental phase (not connect to IGBT), the V_{CE} MONITORING (X2.5; X3.5) must be connected with the EMITTER output (X2.1; X3.1) to avoid possible fault indication and consequent gate signal blocking.

■ “The OUTPUT BUFFER” is responsible for providing +15V/-8V level from the DC/DC inverter, and enhance the control signal from the pulse transformer. The output stage has a MOSFET pair which is able to source/sink up to 8A peak current to/from the gate improving the turn-on/off capability. If these signals do not have sufficient power, the IGBT will not switch properly, and additional losses or even the destruction of the IGBT may occur. According to the application (switching frequency and gate charge of the IGBT), different R_{Gon} and R_{Goff} must be selected. The internal R_{Gon} of the driver is 22Ω , R_{Goff} is 22Ω . Need R_{Gon} can be gained by paralleling relevant resistor on pins J8K8 and J15K15; need R_{Goff} can be gained by paralleling relevant resistor on J9K9 and J16K16.

Please make sure that the total value of R_{Gon} & R_{Goff} not below 2.7 Ω in order to avoid damaging driver.

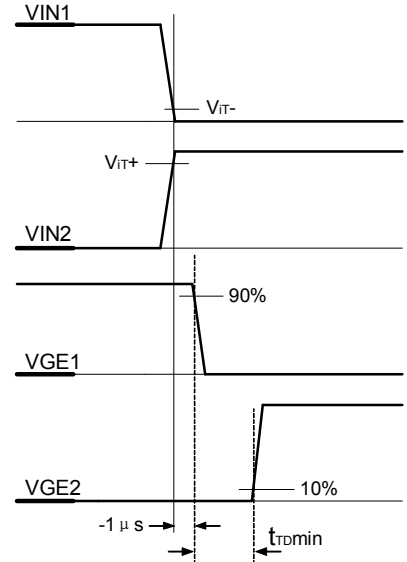


Fig 3 Interlock function

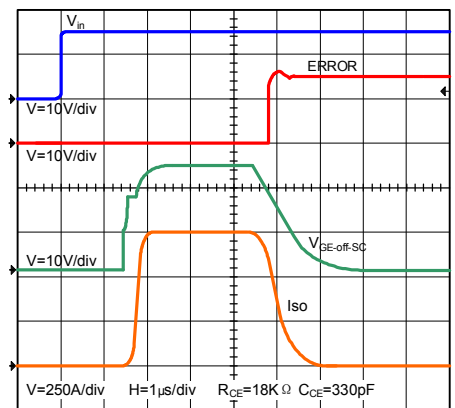


Fig.4 Soft turn-off waveform

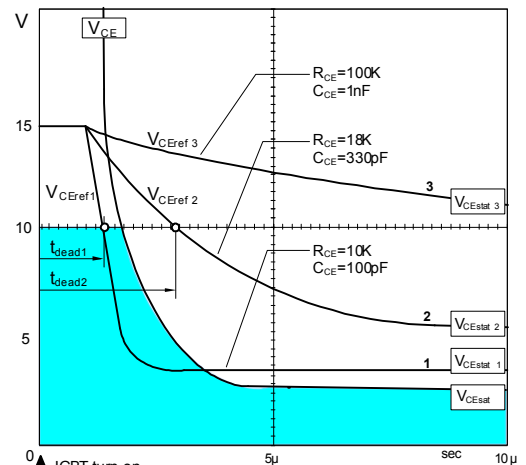


Fig.5 V_{CEref} protection waveform with parameters R_{CE} and C_{CE}

■ Pins J10,K10 and J17,K17 are used for selecting Source Voltage Turn-off Pattern or Source Current Turn-off Pattern, soldering bridge between them makes $I_{Rgoff}=0$. The standard turn-off mode is Source Voltage Turn-off Pattern. Adopting Source current turn-off pattern can improve the switch off rate of IGBTs with 1700V under the condition of $R_{goff}=0$.

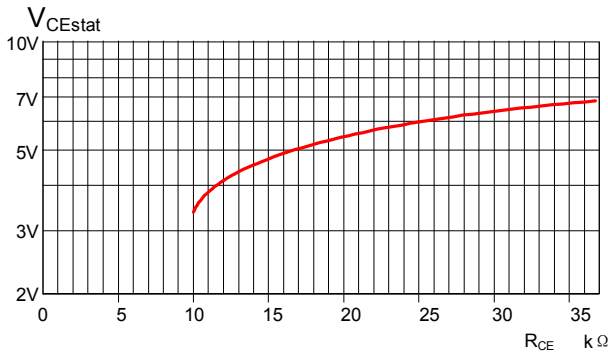


Fig. 6a, V_{CEstat} as function of R_{CE}

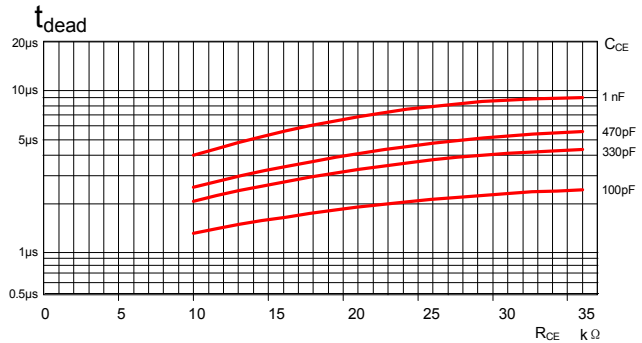


Fig.6b t_{dead} as function of R_{CE} and C_{CE}

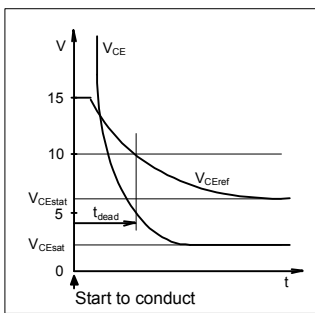


Fig 7a.Usual case

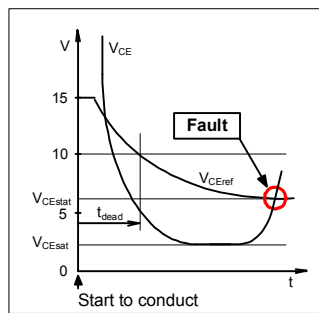


Fig 7b.Short circuit during operation

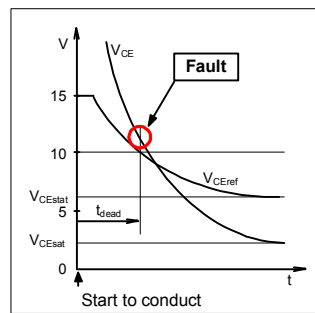


Fig 7c.IGBT turns on too slowly or dead time is too short

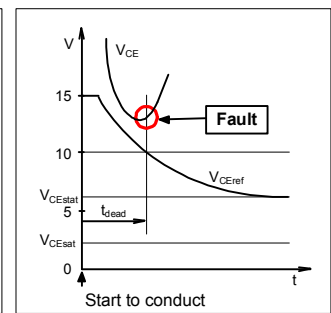


Fig 7d.Short circuit during turn-on

5. Input Interface Criterion

1).Input Signal Level

Input PWM signals can be 15V CMOS/5V TTL(HCMOS) level, active-logic control(high level IGBT switch on). X1.4 is up IGBT controlled signal, while X1.2 is bottom IGBT signal.

2).Error Output

When over-current occurs, driver can cut off IGBT automatically. Fault signals output X1.3 can demand high level active (high level is fault), or output low level active.

When high level active,Pin X1.3 is required to be connected through a pull-up resistor.While low level active, Pin X1.3 need not to connected with pull-up resistor when all drivers can use on error output line. The voltage of pull-up circuit should below 24V, and external power supply should below 6mA(see Fig 8). The standard output error signal is high level active.

3).Error Reset

Install both X1.4 and X1.2 LOW at the same time for more than 5 us, error reset automatically(see Fig 8).

4).Connecting leads between Driver and Control Board

The length between driver and control board should be kept short. If the length is below 50cm, connect with common flat cable is OK (see Fig 9a) .If the length is 50-100cm,only CMOS level can be used for signal transmission,flat cable must have the pairs of conductors twisted or be shielded. If a shielded cable is used, it can be connected to pin X1.1 and solder bridged J20 with K20. The connecting leads between driver and control board is not allowed to more than 1 meter.(see Fig 9b)

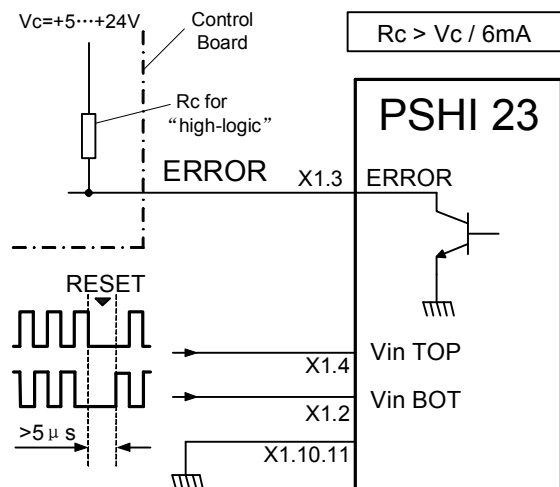


Fig.8 Driver status information ERROR and RESET

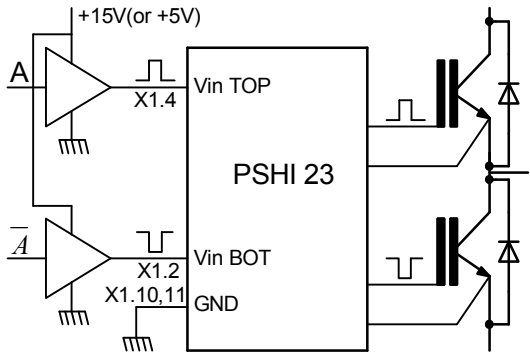


Fig 9a. Connecting PSHI 23 with short cables(<50cm)

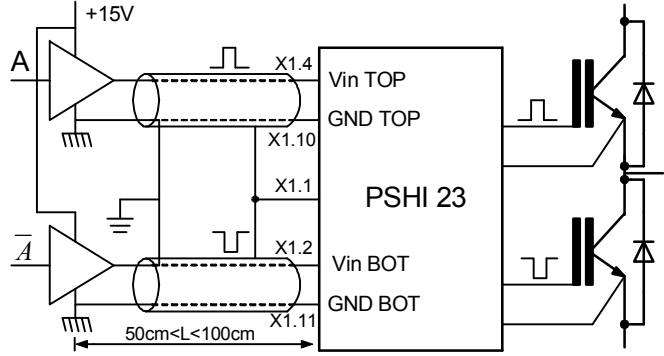


Fig 9b. Connecting PSHI 23 with long cables(50-100cm)

5).Connecting leads between driver and IGBT.

If only connection with low power IGBT, turn-on and turn-off two gate outputs can be done by connecting solder bridged jumper J12,K12 and J19,K19 to IGBT using a gate output cable(see Fig.10). Solder bridging of installed R_{Gon} and R_{Goff} on driver board is highly recommended, and install the gate resistor R_{Gon} and R_{Goff} onto a small piece of PCB near the IGBT gate to avoid the rush rise of temperature on driver surface when high peak current going through gate resistor.The length between driver and IGBT should be as short as possible,flat cable must have the pairs of conductors twisted.

6).Paralleling IGBTs

To get high power output, paralleling IGBTs is recommended. The parallel connection is recommended only by using IGBTs with homogeneous structure, that have a positive temperature coefficient resulting in a perfect current sharing without any external auxiliary element.Care must be considered to reach an optimized circuit and to obtain the total performance of the IGBT:The IGBTs must have independent values of R_{Gon} and R_{Goff} , and an auxiliary emitter resistor R_E as well as an auxiliary collector resistor R_C must also be used.The external resistors R_{Gonx} , R_{Goffx} , R_{EX} (0.5Ω) and R_{CX} (47Ω) should be mounted on an additional circuit board near the paralleled module, and the R_{Gon}/R_{Goff} should be soldering bridged. The cable length between additional circuit board and each IGBT should keep the same(see Fig.11).

The maximum gate charge for PSHI 23 is 4.8uC.

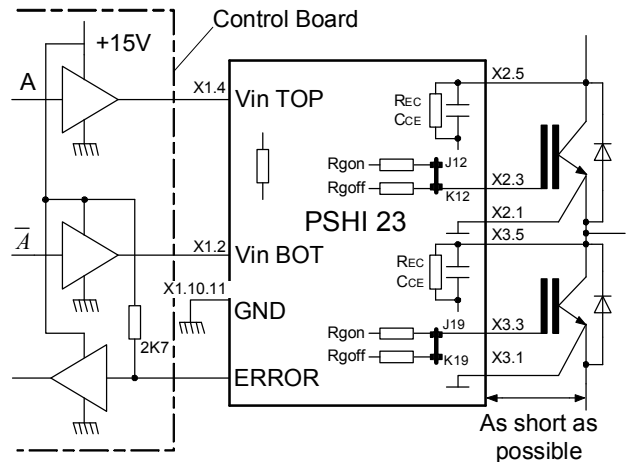


Fig 10.Preferred single IGBT-module standard circuit

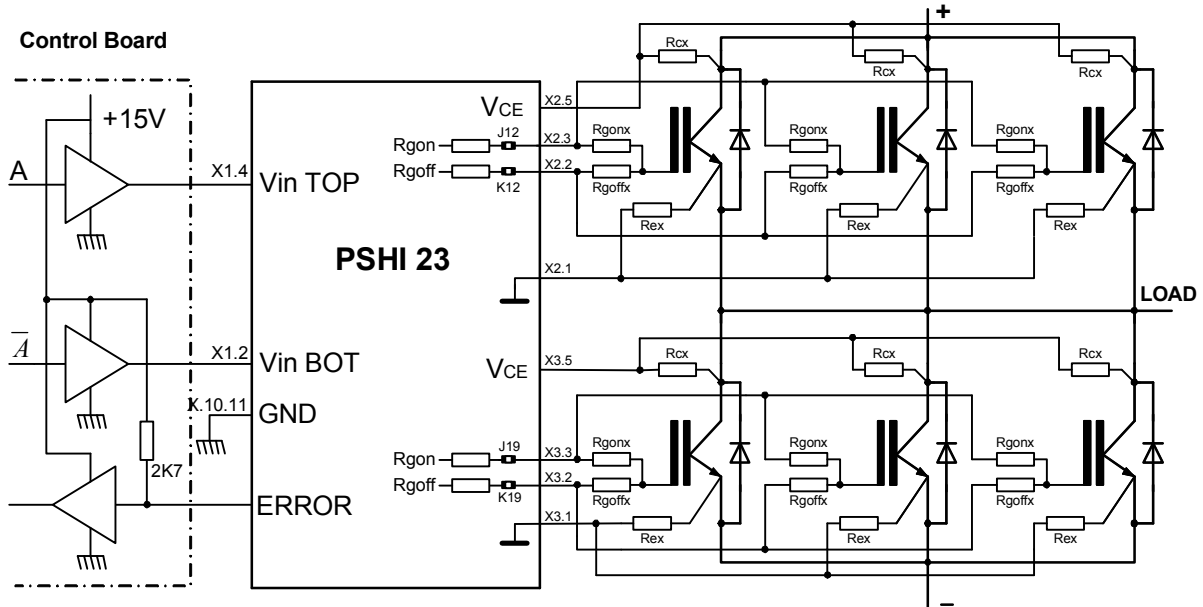


Fig 11.Preferred circuit for paralleled dual IGBT-modules

6. Dimensions and connections of The PSHI 23

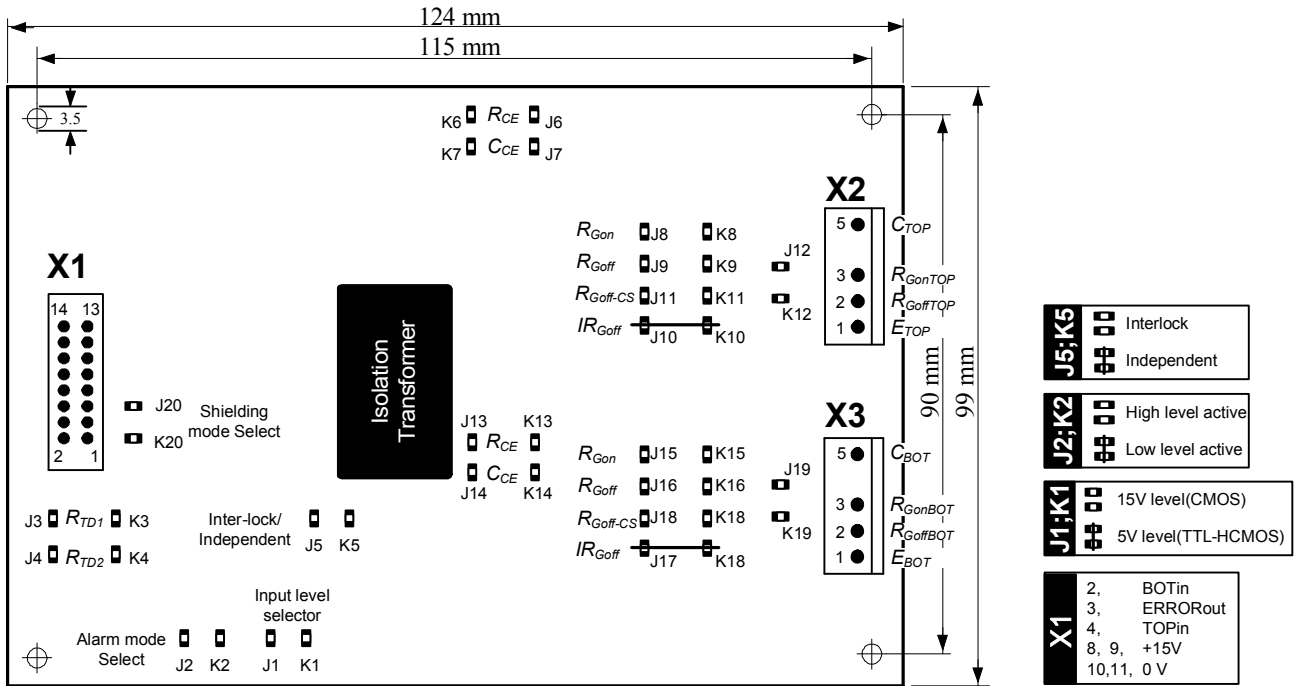


Fig.12 Installation dimensions and pins place instruction

Tab.2 Pins place instruction from J1,K1 to J20,K20

Function	Pin description	Adjustment by factory	Possibilities of functions
Input level selector	J1, K1	not bridged : 15V CMOS	soldering bridged : 5V HCMOS
Error-logic	J2, K2	not bridged : High level active	soldering bridged : Low level active
Dead time	J3, K3 : TOP J4, K4 : BOT	not equipped : 10µs	adjustment according Tab.1
Inter-lock	J5, K5	not bridged : interlock active	soldering bridged:Independent
R _{CE} TOP	J6, K6	not equipped : PSHI2312,18kΩ PSHI2317,36kΩ	adjustment according Fig.6
C _{CE} TOP	J7, K7	not equipped : PSHI2312,330pf PSHI2317,470pf	adjustment according Fig.6
R _{Gon} TOP	J8, K8	not equipped : 22Ω	adjustment automatically
R _{Goff} TOP	J9, K9	not equipped : 22Ω	adjustment automatically
IR _{Goff} TOP	J10, K10	soldering bridged	adjustment automatically
R _{Goff-SC} TOP	J11, K11	not equipped : 22Ω	adjustment automatically
TOP: one IGBT/ paralleled IGBTs	J12, K12	not equipped : 2 cables to gates	soldering bridged:1 cable to gate
R _{CE} BOT	J13, K13	not equipped : PSHI2312,18kΩ PSHI2317,36kΩ	adjustment according Fig.6
C _{CE} BOT	J14, K14	not equipped : PSHI2312,330pf PSHI2317,470pf	adjustment according Fig.6
R _{Gon} BOT	J15, K15	not equipped : 22Ω	adjustment automatically
R _{Goff} BOT	J16, K16	not equipped : 22Ω	adjustment automatically
IR _{Goff} BOT	J17, K17	soldering bridged	adjustment automatically
R _{Goff-SC} BOT	J18, K18	not equipped : 22Ω	adjustment automatically
BOT: one IGBT/ paralleled IGBTs	J19, K19	not equipped : 2 cables to gates	soldering bridged : 1 cable to gates
Shield	J20, K20	not bridged : not connect with GND	soldering bridged : screening to GND

7. Application/Handling

- 1).The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than ($V_s + 0.3V$) or under-0.3V may destroy drivers. Therefore, the signal of control board must be observed for above mentioned demand, and not-used pins should be soldering bridged with GND in order to avoid un-equipped pins. Pay more attention to electrostatic breakdown.
- 2).The connecting leads between the driver and the power module must be as short as possible, and should be twisted.
- 3).Any parasitic inductance should be minimized, turn-off over-voltage can be decreased by different snubber circuit.
- 4).It is important to feed any ERROR back to the control circuit to switch the equipment off immediately in such events.
Repeated turn-on of the IGBT into a short circuit, with a frequency of several kHz, may destroy the device.